ANALYSIS AND PROPOSAL OF AN ISOLATED DC/AC SYSTEM USING THREE-STATE SWITCHING CELL

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***Abstract* – This paper presents an isolated dc/ac system using the three-state switching cell (3SSC). This converter is meant to operate as interface converter for microgrid or stand-alone applications in conjunction with a small power generating units. This system consists in two power processing stages. The first one is a dc/dc boost converter based in the 3SSC and the second one is a classical voltage source inverter (VSI) based in the full bridge inverter. The mentioned cell added in the dc/dc stage allows the use of only two windings in the isolation transformer, as well as, the series connection of only one dc current blocking capacitor to avoid its saturation. Other relevant characteristics of the system are, the blocking voltage across the controlled switches in the dc/dc stage is low, which allows the utilization of lower drain-to-source conduction resistances (R_{DSon}) MOSFETs, and the current through the autotransformer winding is almost continuous minimizing the hysteresis losses on the magnetic core. The operating principle of the proposed system has been analyzed in detail. In order to verify the feasibility of this topology, experimental waveforms are shown for a 1kW assembled prototype.**

***Keywords* – Dc-ac systems, isolated dc/dc converter, three state switching cell.**

I. INTRODUCTION

Nowadays, for economic, technical and environmental reasons there is a trend towards utilization of distributed generation systems in the world. The insertion of distributed generation systems will cause a change of paradigm from centralized electrical generation. It is expected that the utility grid will be formed by a number of interconnected microgrids [1].

This microgrids can be connected to local low-voltage electric power networks, through power conditioning units (i.e., dc/ac isolated or non-isolated systems), which can operate either in grid-connected mode or in stand-alone mode (in this case is added a battery charger and a battery bank).

Distributed power generators that can be used in these systems include wind-turbines, small gas-turbines with direct drive generators, fuel cells or photovoltaic arrays. In all of these cases the same dc/ac system could be used and needs to be controlled to provide high-quality supply waveform to consumers.

The most common configuration used in cited applications is composed by a single-phase approach with lower input voltage levels by employing multi-stage topologies (Fig. 1). A high variety of different topologies were used in the past and described in the literature [2]. In most cases the topologies were characterized by high frequency step-up transformers to perform the necessary high voltage gain.

Regarding the dc-dc converter, in order to reduce the number of stages and increase efficiency and reliability, several approaches used transformers belonging to topologies derived from isolated dc-dc converters like push-pull [3-4], flyback [5-6], two-inductor isolated boost converter without and with autotransformer [7-8] and an isolated boost converter [9] were proposed. A common drawback of such approaches in comparison to others employing a more complex switching scheme is the higher voltage stress across semiconductors.

A further disadvantage inherent to push-pull derived topologies is the necessity of balanced magnetizing mechanisms in order to avoid transformer saturation.

In general, a clear advantage of all isolated approaches is the obtained galvanic insulation and power decoupling. Drawbacks are the lower levels of efficiency due to high frequency switching to reduce transformer size, losses on the transformer itself and increasing complexity.

The proposed dc/ac system in this work is based on the 3SSC [10, 11]. The topology is shown in Fig. 2. Compared to the conventional push-pull converter in the dc/dc stage, the proposed converter presents the following advantages: the 3SSC allows the utilization of only one primary winding that permits to add a dc current blocking capacitor in series connection, in order to avoid the transformer saturation problem; less copper and magnetic core are involved during the transformer assembly; and the moderate leakage inductance of the transformer allows the reduction of the commutation losses of the switches. The autotransformer of the 3SSC has small size, because it is designed for half output power of the converter and for a high magnetic flux density since the current through the windings is almost continuous with low ripple.

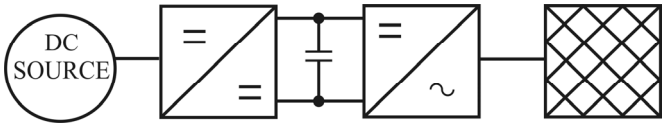


Fig. 1. Common configuration of a single phase dc/ac system used for low input voltage distributed energy source.

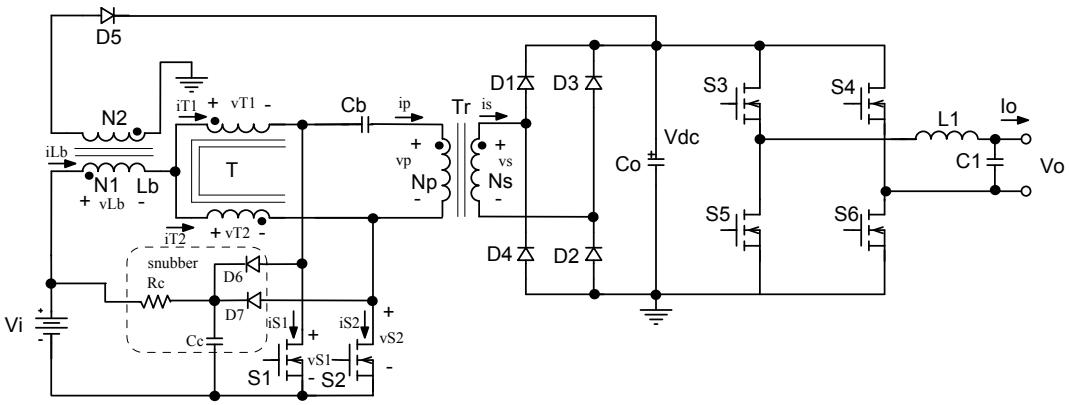


Fig. 2. The proposed dc/ac system using the three-state switching cell.

The inverter consists in a classical VSI based on full-bridge inverter. In this paper the major emphasis is given to the high gain converter, because the inverter stage it is well known.

II. ANALYSIS OF THE ISOLATED DC-DC CONVERTER STAGE USING 3SSC

A. Description of the Circuit

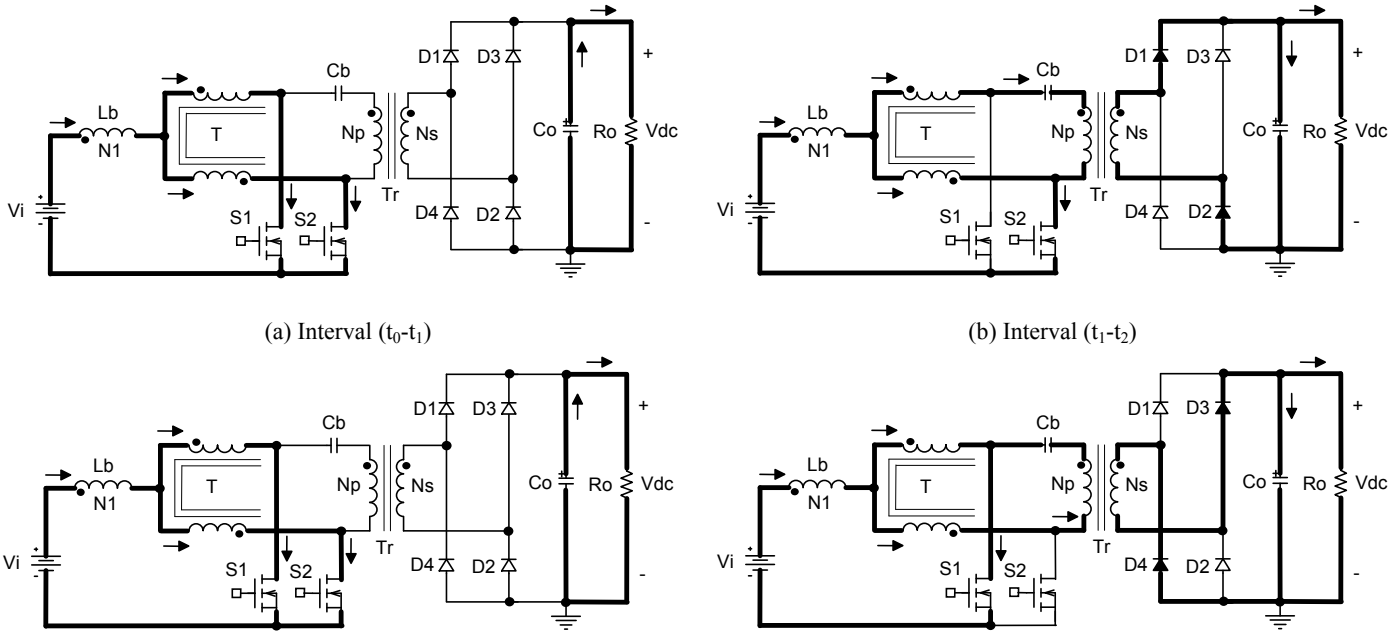
The proposed converter shown in Fig. 2 is composed by the following devices: a storage coupled inductor L_b with turns number N_1 and N_2, an autotransformer T with unitary turns ratio, one dc current blocking capacitor C_b, an isolated transformer T_r with turns number N_p and N_s, two controlled switches S_1 and S_2, four rectifier diodes D_1-D_4, one filter capacitor C_o, one flyback diode D_5, and load resistor R_o. A small clamp circuit is also shown between dashed lines and is used in the controlled switches against overvoltages.

B. Principle of Operation

The proposed converter is analyzed with overlapping of control signals or with duty cycle higher than 0.5, operating in continuous conduction mode (CCM). In this analysis, all the components involved in the converter are considered ideals. During one commutation period it presents four operating intervals that are described as follows. The key waveforms of the corresponding intervals are shown in Fig. 4.

• ***Interval (t_0, t_1):*** The switches S_1 and S_2 are turned on. The input voltage is applied to the storage inductor L_b, and as consequence the current increases linearly through it. The autotransformer T is short-circuited because the resultant magnetic flux of the core is null. The diodes D_1-D_4 are reverse biased. The load resistor is feed by the filter capacitor C_o. This stage is shown in Fig. 3.a and it finishes when switch S_1 is turned off.

• ***Interval (t_1, t_2):*** In this interval the switch S_2 remains turned on. The voltage across switch S_1 is equal to the primary side voltage of the isolation transformer T_r. The diodes D_1 and D_2 are directly biased. The energy stored in the inductor in the first interval, as well as, the energy from the voltage source are transferred to the filter capacitor C_o and resistor R_o. The resultant circuit from this operating stage is shown in Fig. 3.b.



(a) Interval (t_0-t_1)

(b) Interval (t_1-t_2)

(c) Interval (t_2-t_3)

(d) Interval (t_3-t_4)

Fig. 3. Topological stages of the dc/dc converter stage.

• ***Interval (t_2, t_3):*** This interval is similar to the first one, where switches S_1 and S_2 are turned-on, and the energy is again stored in the inductor L_b. The diodes D_1-D_4 are reverse biased. It is finished when switch S_2 is turned-off. This stage is shown in Fig. 3.c.

• ***Interval (t_3, t_4):*** During this interval, the switch S_1 remains turned-on. The voltage across switch S_2 is equal to the voltage across primary side of the isolated transformer T_r. The rectifier diodes D_3 and D_4 are directly biased. The energy stored in the inductor L_b during the third stage, as well as, the energy from the voltage source are transferred to the filter capacitors C_o and load resistor R_o. This interval is shown in Fig. 3.d.

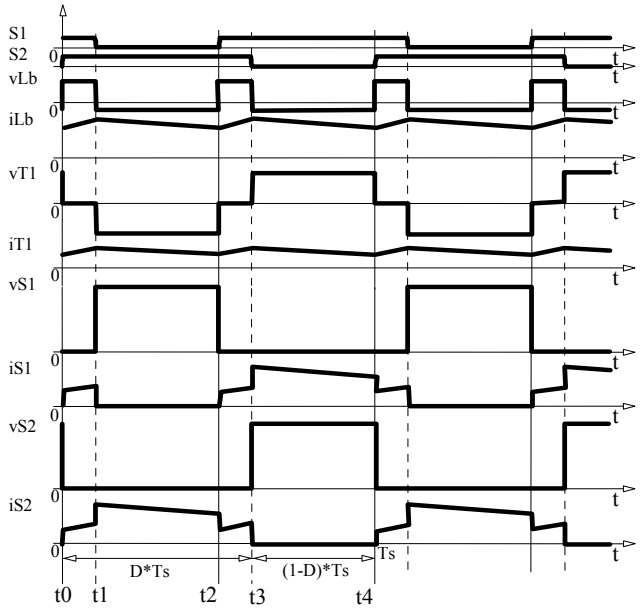


Fig. 4. Key waveforms of the proposed converter.

C. Voltage Static Gain

The ideal voltage static gain of the converter and the transformer turns ratio of the transformer T_r is given respectively by

$$Gv = \frac{Vi}{V_{dc}} = \frac{a}{(1-D)}, \tag{1}$$

$$a = \frac{Ns}{Np}, \tag{2}$$

where V_{dc} is the dc link voltage, Vi is the input voltage, D is the duty cycle of the converter, Ns is the secondary turns number of the transformer T_r, and Np is the primary turns number of the transformer T_r.

The voltage static gain curves as function of the duty cycle, taken as parameter of transformer turns ratio a, are shown in the Fig. 5.

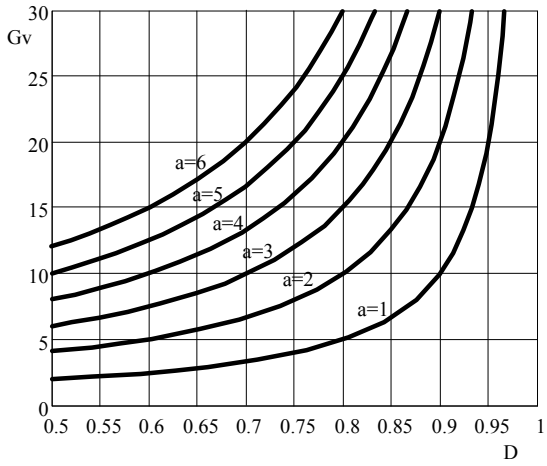


Fig. 5. Normalized voltage static gain taken as parameter transformer turns ratio.

D. Inductor Design

The current ripple on the inductor is given by

$$\Delta I_{Lb} = \frac{V_{dc}(2D-1)(1-D)}{2af_sL_b}, \tag{3}$$

where ΔI_{Lb} is the current ripple on the inductor L_b and f_s is the switching frequency of the converter.

Rearranging (3), the normalized current ripple in the inductor is given by

$$\overline{\Delta I_{Lb}} = \frac{af_sL_b\Delta I_{Lb}}{V_{dc}} = \frac{(2D-1)(1-D)}{2}, \tag{4}$$

The Fig. 6, which is obtained using (4), shows the normalized current ripple on the inductor as a function of the duty cycle.

Therefore, it is possible to conclude that the maximum current ripple on the inductor occurs when the duty cycle is equal to 0.75 and the normalized current ripple is equal to 0.063.

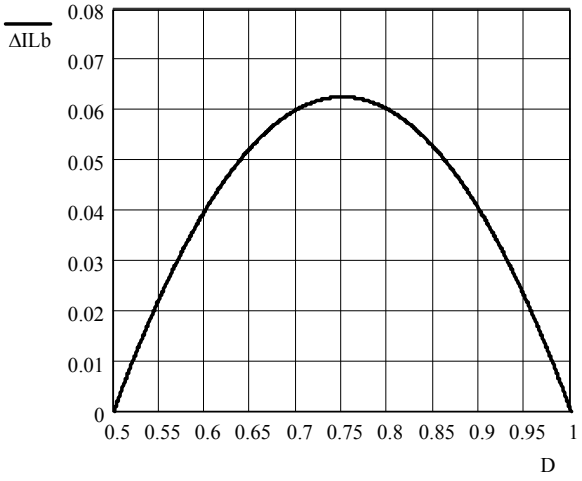


Fig. 6. Normalized ripple current on the inductor L_b.

Thus, for a given value to the current ripple, it is possible to determine the inductor value as

$$L_b = \frac{V_{dc}}{16af_s\Delta I_{Lb}}, \tag{5}$$

The turns number N_1 of the storage inductor L_b can be determined by

$$N_1 = \frac{L_b I_{Lb\_pk}}{A_e B_{max}}. \quad (6)$$

where I_{Lb_pk} is the inductor peak current, A_e is the core cross section, and B_{max} is the maximum flux density.

An auxiliary winding with N_2 turns number and opposed polarity is coupled to the storage inductor L_b with N_1 turns number. This auxiliary winding is used to discharge the storage inductor L_b when occurs an open circuit problem in the primary side of the transformer. Otherwise, high damage overvoltages may occur mainly in the controlled switches.

From the flyback converter criterion operating in the continuous conduction mode is determined the turns number N_2 by

$$N_2 \geq \frac{(1-D)}{D}\frac{V_{dc}}{Vi} N_1. \quad (7)$$

E. Autotransformer Design

The high frequency autotransformer T must be designed for half active output power, and high magnetic flux density, B, because the current through the windings is continuous and with low ripple. The autotransformer turns ratio must be unitary. Thus,

$$P_T = \frac{Po}{2}, \quad (8)$$

where P_T is the active power processed by the autotransformer T, and Po is the output power of the converter.

F. Transformer Design

The isolated high frequency transformer Tr must be designed for the total active output power. The transformer turns ratio is taken from (1) and from characteristic curves shown in Fig. 5.

In order to reduce Eddy currents losses in the core, so as leakage inductance, the winding layers of the primary and the secondary of the transformer are mounted as the sandwich assembly [12]. The power of the isolation transformer is determined by

$$P_{Tr} = Po. \quad (9)$$

G. DC Current Blocking Capacitor

The dc current blocking capacitor avoids the saturation problem of the isolated transformer. This capacitor must be made of polypropylene due to its low internal resistance and AC polarity, because the total load current circulates through it. Considering a peak to peak voltage variation, and current circulation through it, the capacitance of the capacitor C_b can be determined by

$$C_b = \frac{I_{Lb\_avg}(1-D)}{2 f_s \Delta V_{Cb}}, \quad (10)$$

where ΔV_{Cb} is the peak to peak voltage variation across capacitor defined by

$$\Delta V_{Cb} = \xi \frac{V_{dc}}{a}, \quad (11)$$

I_{Lbavg} is the average current circulating in the storage inductor L_b, ξ is an absolute value lower than one relative to the primary side voltage of the transformer T_r (in practical applications can be chosen between 0.05 to 0.15).

H. Current and Voltage Stresses in Switches S_1 and S_2

The root-mean-square (rms) current through the switch S_1 that is equal to the switch S_2, considering a small current ripple through the storage inductor L_b, can be determined by

$$I_{S1\_rms} \cong I_{Lb\_avg}\sqrt{\frac{3}{4}-\frac{D}{2}}. \quad (12)$$

The maximum voltage across of switches S_1 and S_2, without considering the parasitic inductances that causes overvoltages, is almost equal to the primary side voltage of the isolated transformer. The voltage across the switches is dependent of the leakage inductance of the transformer T_r and other parasitic inductances. Therefore, a snubber circuit is recommended to limit such value. The maximum voltage stress across the controlled switches is given by

$$V_{S1} = V_{S2} \geq \frac{V_{dc}}{a}. \quad (13)$$

I. Current and Voltage Stresses in Diodes D_1-D_4

The average current through the rectifier diodes D_1-D_4 is given by

$$I_{D1\_avg} \cong \frac{Io}{2}. \quad (14)$$

The maximum reverse voltage across of the rectifier diodes D_1-D_4, without considering overvoltages, is equal to the output voltage that is expressed by

$$V_{D1} \geq V_{dc}. \quad (15)$$

J. Output Filter Capacitor Design

The capacitance of the output filter capacitor, for purely resistive load, can be determined by

$$Co \geq \frac{Io(2D-1)}{2\Delta V_{dc} f_s}. \quad (16)$$

III. VOLTAGE SOURCE INVERTER STAGE

In order to perform dc/ac conversion, a classical voltage source full-bridge inverter is connected to the dc link capacitors. The topology is shown in Fig. 7.

In order to control the output voltage, a sinusoidal PWM control with unipolar voltage switching was applied. To protect the switches against overvoltages, a decoupling polypropylene capacitor was placed in parallel with each inverter leg.

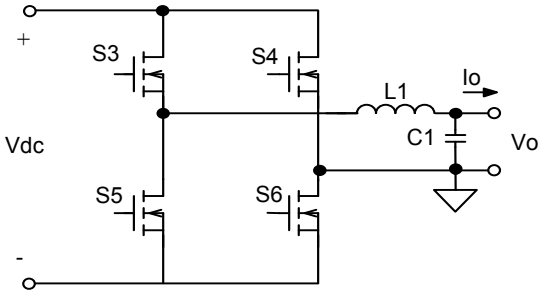


Fig. 7 Inverter stage schematic.

The filter inductance is obtained from the inductor voltage equation. The design considers purely resistive load, and the

angle of the fundamental input voltage across the LC filter is θ=ωt=π/2 [12]. The filter inductance is given by

$$L_1 \cong \frac{\left(V_{dc} - \sqrt{2}V_o\right)ma}{2f_s\Delta IL_1} \quad (17)$$

where, ma is the modulation index and ΔIL_1 is the current ripple on the inductor L_1.

The resonance frequency of the output LC filter applying unipolar voltage switching technique is given by expression (18) [12],

$$f_o \le \frac{2f_s}{10} = \frac{1}{2\pi\sqrt{L_1C_1}} \quad (18)$$

IV. SIMPLIFIED DESIGN EXAMPLE

A. Preliminary Specifications

The design specifications of the proposed dc/ac system using three-state switching cell are shown in Table I. The switching frequency for the all stages is assumed f_s=25kHz. For this design and application batteries were used to simulate the input voltage source

TABLE I
Isolated dc/ac system Specifications

Input Voltage Range	*Vi*	42 - 54 [V_{DC}]
Output Power	*Po*	1 [kW]
Dc Link Voltage	*Vdc*	400 [V]
Output voltage	*Vo*	220 [V_{AC}]
Output frequency	f_o	60 [Hz]

The design parameters of the dc/ac system stages are listed in Tables II and III.

TABLE II
Design Parameters of dc/dc converter Stage

Transformer turns ratio	$a = N_s/N_p = 3$
Maximum duty cycle	$D_{max} = 0.70$
Maximum boost inductor current ripple	$\Delta I_{Lb} = 0.18 I_{Lb\_avg}$
Output voltage ripple	$\Delta V_{DC} = 0.01 V_{DC}$
Dc current blocking capacitor coefficient	$\xi = 0.1$

TABLE III
Design Parameters of dc/ac converter Stage

Modulation index	$ma = 0.78$
Filter inductor ripple current	$\Delta IL_1 = 1.0\text{A}$

B. Design Procedure of the dc/dc Converter

The boost inductance and the dc link capacitance are obtained substituting the dc/dc stage design parameters in (5) and (16), respectively. Yields,

$$L_b = \frac{V_{dc}}{16af_s\Delta I_{Lb}} = 70\mu\text{H},$$

$$Co \ge \frac{Io(2D-1)}{2\Delta V_{dc}f_s} = 5\mu\text{F} \text{ (for purely resistive load).}$$

Considering the inverter as load, two electrolytic capacitors of 470μF/450V in parallel was adopted on the dc-link.

C. Design Procedure of the Voltage Source Inverter

The filter inductance is obtained from (17). Substituting the design parameters in (17) gives

$$L_1 \cong \frac{\left(V_{dc} - \sqrt{2}V_o\right)ma}{2f_s\Delta IL_1} = 1.4m\text{H}.$$

Rearranging C_1 of the equation (18), and substituting the design values, the capacitance value is equal to

$$C_1 = \frac{25}{\left(2\pi f_s\right)^2 L_1} = 0.72\mu F.$$

Thus, the inverter output filter capacitance must be greater than $C_1 \ge 0.72\mu$F. The prototype was implemented with a metalized polypropylene capacitor rated at 10μF/250V_{ac}.

V. EXPERIMENTAL RESULTS

In order to verify the feasibility and performance of the proposed isolated dc/ac system, which was assembled with the parameters obtained in the Section IV (devices are listed in Tables IV and V), a laboratory prototype was implemented and evaluated.

The experimental results consist of relevant voltage and current waveforms, and also efficiency.

TABLE IV
Experimental Parameters of the Implemented dc/dc Converter

Diodes $D_1 - D_5$	HFA15PB60
Boost Inductor L_b	L_b = 70μH Core NEE-55/28/21 (Thornton Ipec) N1= 17 turns N2=80 turns
Dc link Capacitors C_o	2 x 470μF / 450V (electrolytic)
Blocking Capacitor C_b	10uF/250V (polypropylene)
Switches S_1 - S_2	IRFP4227
High Frequency Transformer T_r	Core NEE-65/26 (Thornton Ipec) Np=17 turns Ns=51 turns
High Frequency Autotransformer *T*	Core NEE-42/20 (Thornton Ipec) NT1 = NT2 = 19 turns
Clamp circuit components	D_6,D_7 (MUR460) C_c (470nF/400V) Rc (10kΩ / 5W)

TABLE V
Experimental Parameters of the Implemented dc/ac Converter

Output Filter Inductor L_1	L_1 = 1.4mH Core NEE-55/28/21 (Thornton Ipec) N_{L1}= 71 turns
Output Filter Capacitor C_o	10μF / 250V_{ac} (polypropylene)
Switches S_3 - S_6	IXFX44N60

A. Experimental Waveforms

The experimental waveforms shown in Figs. 8-17 were carried for nominal input voltage level.

Fig. 8 shows the measured input voltage *Vi* and current through the boost inductor L_b. As can be seen, the current drawn by the proposed converter presents a low current ripple, suitable for battery powered applications or fuel cell applications, where its requirement is relevant to improve its useful lifetime. It's also important to note that the current ripple frequency is double of the switching frequency.

Figs. 9 and 10 shows the voltage and current through the autotransformer windings. These waveforms are similar that concludes that a good current balance with very low current ripple is achieved.

Fig. 11 shows drain to source voltage and drain current in the switch S_1. As can be seen, the primary switch presents lower voltage stress that could be enhanced if the printed circuit board layout were optimized. Thus, the primary switches voltage specification compared to the conventional isolated boost converters could be significantly reduced. The typical voltage rating of primary switches in isolated boost converters is commonly rated at 2-3 times of the maximum input voltage [13].

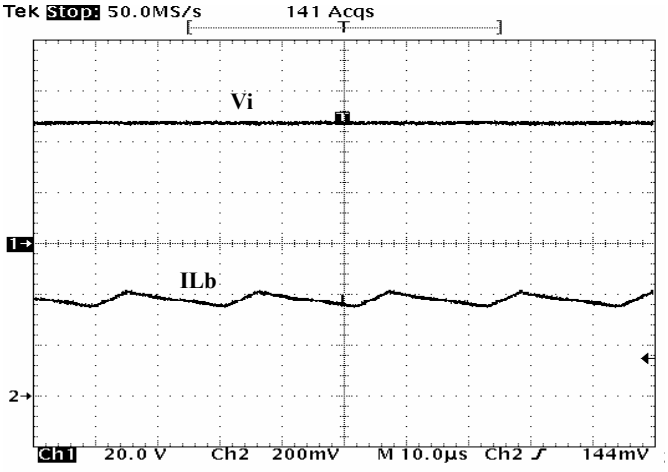


Fig. 8. Input voltage and current through the inductor Lb.
(20V/div.; 10A/div.; 10us/div.)

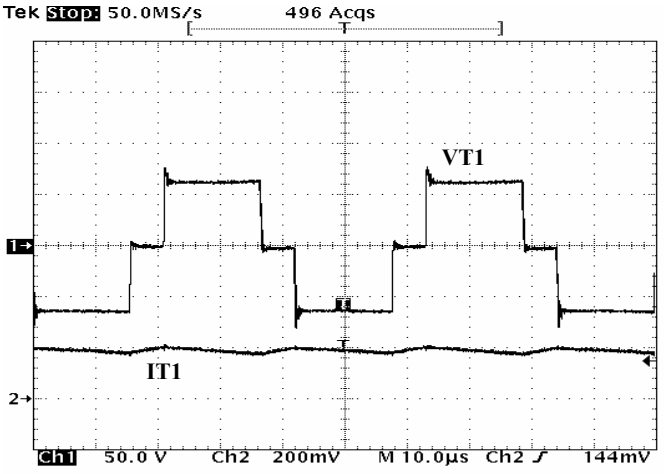


Fig. 9. Voltage and current through the autotransformer winding 1.
(50V/div.; 10A/div.; 10us/div.)

Other parameter that must be optimized is the leakage inductance of the isolated transformer, in order to avoid voltage spikes across the controlled switches. The leakage inductance obtained in the assembly using optimized transformer construction techniques was approximately 1,5uH, and then a small clamp circuit were required and used for switches protection.

The commutation detail of the Fig. 11 during the switch S_1 turn-on and turn off are shown in Fig. 12 and 13, respectively. As can be seen, the switch presents an almost suitable commutation contributing to the switching losses reduction.

Figs. 14 and 15 shows the voltages and currents through the primary side and secondary side of the isolated transformer T_r, respectively. It can be seen that the DC component of the primary side current is eliminated using the blocking capacitor C_b.

The output voltages and currents of the inverter are shown in Figs. 16 and 17, where a high quality sinusoidal voltage waveform is obtained, independently of the load characteristic (linear and non-linear load).

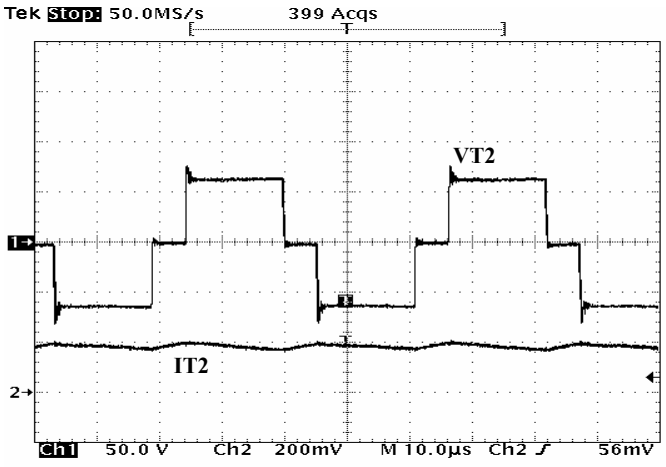


Fig. 10. Voltage and current through the autotransformer winding 2.
(50V/div.; 10A/div.; 10us/div.)

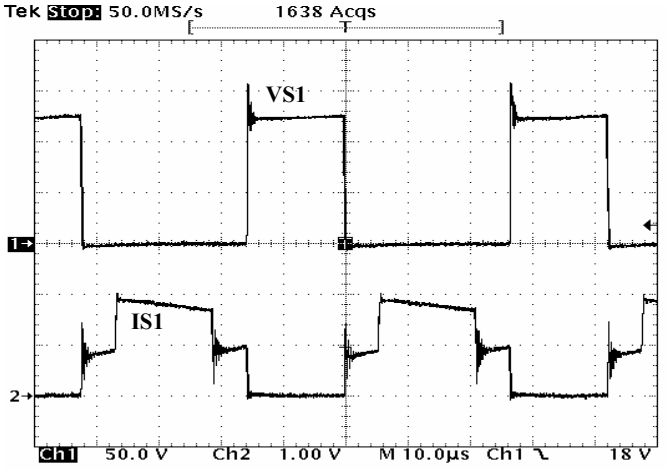


Fig. 11. Voltage and current through switch S_1.
(50V/div.; 10A/div.; 10us/div.)

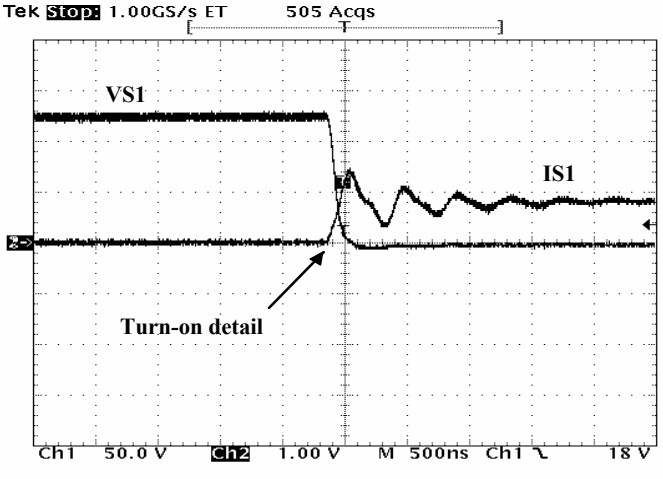


Fig. 12. Turn-on switching detail of the switch S_1.
(50V/div.; 10A/div.; 500ns/div.)

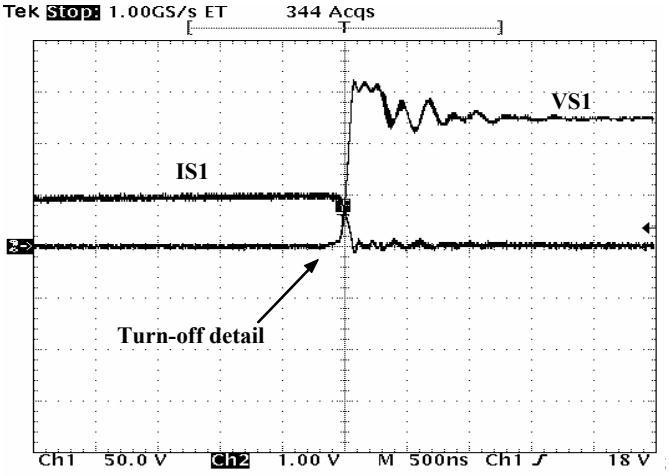


Fig. 13. Turn-off switching detail of the switch S_1.
(50V/div.; 10A/div.; 500ns/div.)

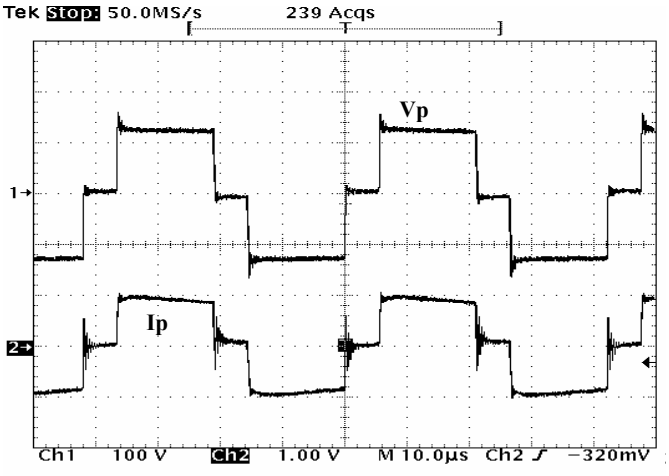


Fig. 14. Primary transformer voltage and current.
(100V/div.; 10A/div.; 10us/div.)

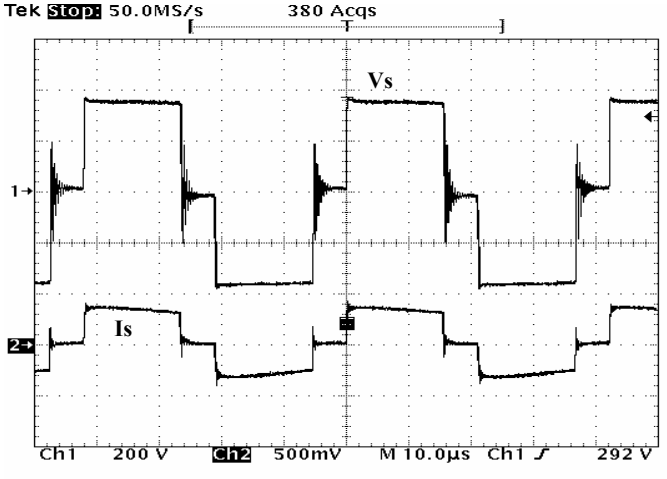


Fig. 15. Secondary transformer voltage and current.
(200V/div.; 5A/div.; 10us/div.)

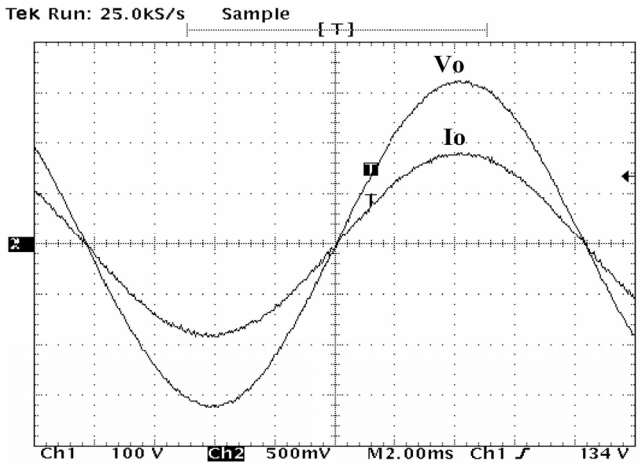


Fig. 16. Output voltage and current of the inverter for linear load.
(Ch1:100V/div., Ch2:5A/div.; 2ms/div.)

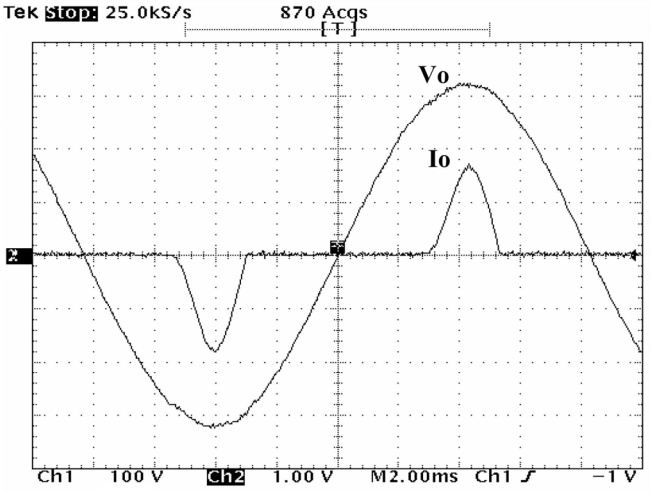


Fig. 17. Output voltage and current of the inverter for nonlinear load condition. (Ch1:100V/div., Ch2:10A/div.; 2ms/div.)

B. Experimental Curves

The experimental efficiency curve was achieved for the worst operation condition when the input voltage was set in 42V for full output power condition.

Fig. 18 presents the measured converter efficiency curve as a function of the output power. Accordingly to this graph evaluation, this converter presented a good efficiency that can be optimized if MOSFETs with lower on-state-resistance were used.

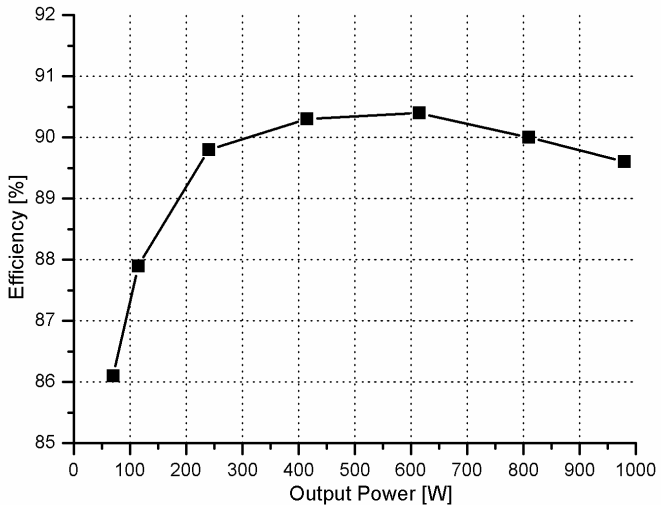


Fig. 18. Measured efficiency of the dc/ac system as function of the output power.

VI. CONCLUSION

In this paper was presented a feasible isolated dc/ac system based on the three-state cell (3SSC). Accordingly to the obtained experimental results, the major features that are important to emphasize are:

- The lower blocking voltages across the controlled switches of the dc/dc converter, which allows the utilization of MOSFETs switches with lower drain-to-source resistances;
- The dc current across isolated transformer could be eliminated using blocking capacitor, and the reasonable leakage inductance value of the isolated transformer is suitable to improve the commutation process of the controlled switches;
- The inverter stage presents sinusoidal output voltage when supplying linear or nonlinear loads;
- Tests results from a 1kW experimental prototype showed that the proposed configuration may be a viable solution for isolated or non-isolated systems operating with low dc input voltage level;
- High efficiency of the converter was obtained (up to 90%) for a full load condition operating at lower input voltage level.

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