A New Isolated DC-DC Boost Converter using Three-State Switching Cell

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***Abstract*-In this paper, a new isolated DC-DC boost converter based on three-state switching cell (3SSC) is proposed. The mentioned cell allows the use of only two windings in the isolation transformer, as well as, the series connection of only one DC current blocking capacitor to avoid its saturation. Other relevant characteristics of the converter are, the blocking voltage across the controlled switches is low, which allows the utilization of lower drain-to-source conduction resistances (RDSon) MOSFETs, and the current through the autotransformer winding is almost continuous minimizing the hysteresis losses on the magnetic core. In this way, the efficiency of the proposed converter is high, and it is recommended for the development of power supplies using low voltage sources commonly found on renewable energy conversion systems and batteries. The converter was analyzed in overlapping of the control signals or duty cycle higher than 0.5 operating in continuous conduction mode (CCM). In order to verify the feasibility of this topology; principle of operation, theoretical analysis, and experimental waveforms are shown for a 1kW assembled prototype.**

I. INTRODUCTION

When the desired application needs to raise a low level input voltage, commonly presented in batteries, photovoltaic solar panels, fuel cells and small wind generators (12Vdc to 125Vdc), to high output DC bus voltage (300Vdc – 400Vdc) required in voltage source inverters (VSI) for applications such as power supply systems, motor drives, etc, the classical current fed DC-DC push-pull converter is commonly the first choice.

The conventional push-pull converter was studied detailed in [1]. The advantages of the push-pull converter are: the topology is suitable for low input voltage application because is involved only one controlled switch in series during energy storage or energy transfer, the switches are referenced to the same potential that improves its gating drive circuit. As disadvantages are: the leakage inductance of the isolated transformer may causes overvoltages stresses across the controlled switches during commutation, and the asymmetrical construction of the transformer and asymmetrical PWM pulses of the control circuit causes saturation problems to the transformer.

The topologies presented in [2-3] are modified push-pull converters based on the non-isolated Weinberg converter. To improve its efficiency and to minimize voltage stresses on the controlled devices, non-dissipative auxiliary circuits were added. Also, others modified push-pull converters with soft switching were proposed in [4-7].

A two-inductor isolated boost converter without and with autotransformer were presented in [8-9]. They operate as an interleaved boost converter. As relevant features of the converter is that the input current of the voltage source is non-pulsating with low ripple, and the maximum voltage stress across the switches is fixed to the primary side voltage of the isolating transformer.

In [10] was implemented an isolated boost converter that exhibits as advantages non parasitic voltage ringing across all of semiconductor devices on the primary and secondary sides of the transformer.

The proposed converter in this work is based on the three-state switching cell (3SSC) [11]. The topology is shown in Fig. 1. Compared to the conventional push-pull converter, the proposed converter presents the following advantages: the 3SSC allows the utilization of only one primary winding that permits to add a DC current blocking capacitor in series connection, in order to avoid the transformer saturation problem; less copper and magnetic core are involved during the transformer assembly; and the moderate leakage inductance of the transformer allows the reduction of the commutation losses of the switches. The autotransformer of the 3SSC has small size, because it is designed for half output power of the converter and for a high magnetic flux density since the current through the windings is almost continuous with low ripple.

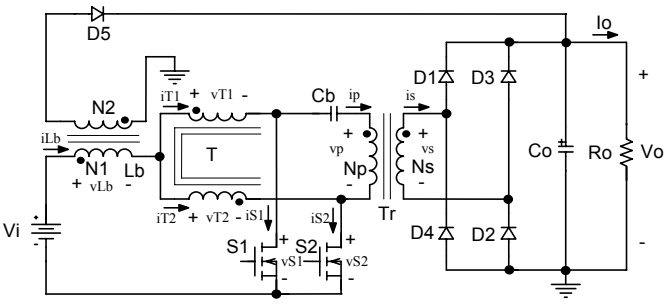


Fig. 1. Proposed isolated DC-DC boost converter using 3SSC topology.

II. PROPOSED ISOLATED DC-DC CONVERTER USING 3SSC

A. Description of the Circuit

The proposed converter shown in Fig. 1 is composed by the following devices: a storage coupled inductor L_b with turns number N_1 and N_2, an autotransformer T with unitary turns ratio, one DC current blocking capacitor C_b, an isolated transformer T_r with turns number N_p and N_s, two controlled switches S_1 and S_2, four rectifier diodes D_1-D_4, one filter capacitor C_o, one flyback diode D_5, and load resistor R_o.

B. Principle of Operation

The proposed converter is analyzed with overlapping of control signals or with duty cycle higher than 0.5, operating in continuous conduction mode (CCM). In this analysis, all the components involved in the converter are considered ideals. During one commutation period it presents four operating intervals that are described as follows. The key waveforms of the corresponding intervals are shown in Fig. 3.

• ***Interval (t_0, t_1):*** The switches S_1 and S_2 are turned on. The input voltage is applied to the storage inductor L_b, and as consequence the current increases linearly through it. The autotransformer T is short-circuited because the resultant magnetic flux of the core is null. The diodes D_1-D_4 are reverse biased. The load resistor is feed by the filter capacitor C_o. This stage is shown in Fig. 2.a and it finishes when switch S_1 is turned off.

• ***Interval (t_1, t_2):*** In this interval the switch S_2 remains turned on. The voltage across switch S_1 is equal to the primary side voltage of the isolation transformer T_r. The diodes D_1 and D_2 are directly biased. The energy stored in the inductor in the first interval, as well as, the energy from the voltage source are transferred to the filter capacitor C_o and resistor R_o. The resultant circuit from this operating stage is shown in Fig. 2.b.

• ***Interval (t_2, t_3):*** This interval is similar to the first one, where switches S_1 and S_2 are turned-on, and the energy is again stored in the inductor L_b. The diodes D_1-D_4 are reverse biased It is finished when switch S_2 is turned-off. This stage is shown in Fig. 2.c.

• ***Interval (t_3, t_4):*** During this interval, the switch S_1 remains turned-on. The voltage across switch S_2 is equal to the voltage across primary side of the isolated transformer T_r. The rectifier diodes D_3 and D_4 are directly biased. The energy stored in the inductor L_b during the third stage, as well as, the energy from the voltage source are transferred to the filter capacitors C_o and load resistor R_o. This stage is shown in Fig. 2.d

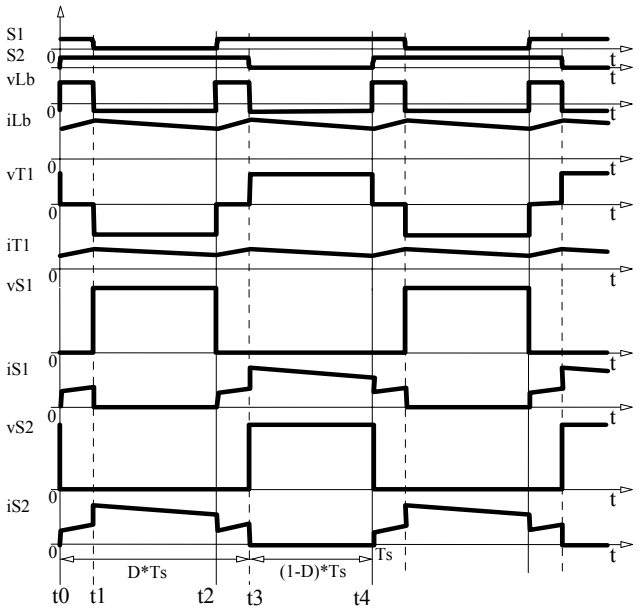
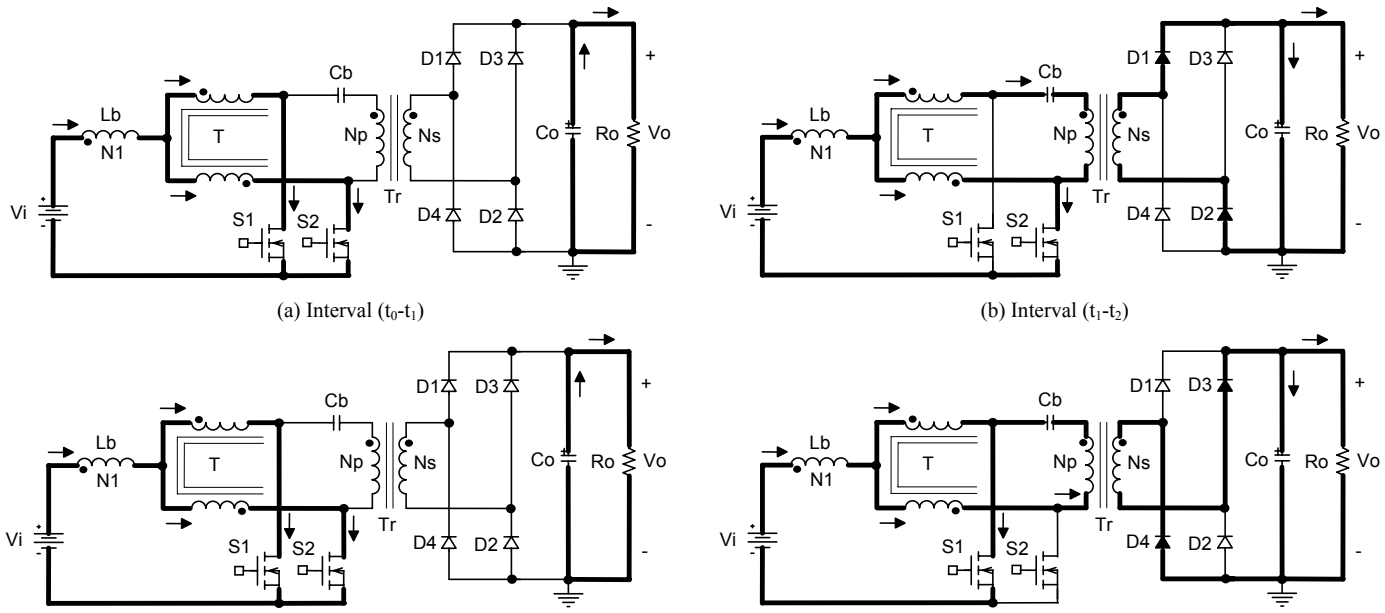


Fig. 3. Key waveforms of the proposed converter.



(a) Interval (t_0-t_1)

(b) Interval (t_1-t_2)

(c) Interval (t_2-t_3)

(d) Interval (t_3-t_4)

Fig. 2. Operation stages of the proposed converter.

III. Analysis of The Proposed Converter

A. Voltage Static Gain

The ideal voltage static gain of the converter and the transformer turns ratio of the transformer T_r is given respectively by

$$Gv = \frac{Vi}{Vo} = \frac{a}{(1-D)}, \tag{1}$$

$$a = \frac{Ns}{Np}, \tag{2}$$

where Vo is the output voltage, Vi is the input voltage, D is the duty cycle of the converter, Ns is the secondary turns number of the transformer T_r, and Np is the primary turns number of the transformer T_r.

The voltage static gain curves as function of the duty cycle, taken as parameter of transformer turns ratio a, are shown in the Fig. 4.

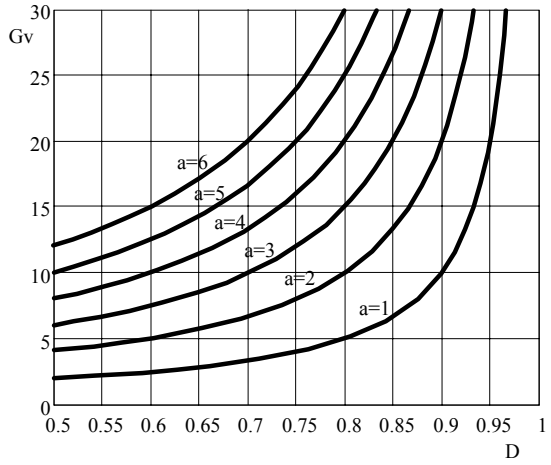


Fig. 4. Normalized voltage static gain taken as parameter transformer turns ratio.

B. Inductor Design

The current ripple on the inductor is given by

$$\Delta I_{Lb} = \frac{Vo\,(2D-1)(1-D)}{2af_sL_b}, \tag{3}$$

where ΔI_{Lb} is the current ripple on the inductor L_b and f_s is the switching frequency of the converter.

Rearranging (3), the normalized current ripple in the inductor is given by

$$\overline{\Delta I_{Lb}} = \frac{af_sL_b\Delta I_{Lb}}{Vo} = \frac{(2D-1)(1-D)}{2}. \tag{4}$$

The Fig. 5, which is obtained using (4), shows the normalized current ripple on the inductor as a function of the duty cycle.

Therefore, it is possible to conclude that the maximum current ripple on the inductor occurs when the duty cycle is equal to 0.75 and the normalized current ripple is equal to 0.063.

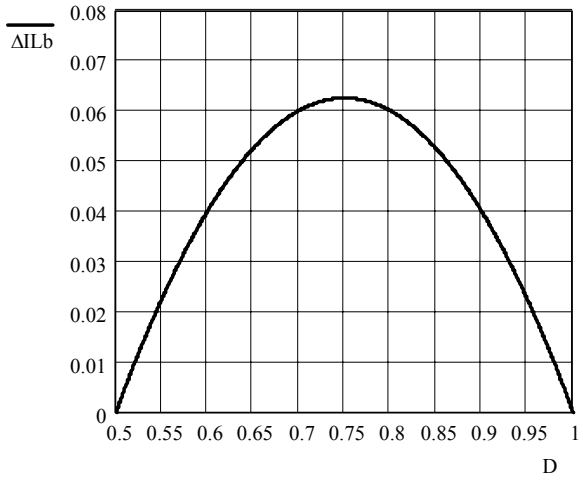


Fig. 5. Normalized ripple current on the inductor L_b.

Thus, for a given value to the current ripple, it is possible to determine the inductor value as

$$L_b = \frac{Vo}{16af_s\Delta I_{Lb}}. \tag{5}$$

The turns number $N1$ of the storage inductor L_b can be determined as

$$N_1 = \frac{L_bI_{Lb\_pk}}{A_eB_{max}}. \tag{6}$$

where I_{Lb_pk} is the inductor peak current, A_e is the core cross section, and B_{max} is the maximum flux density.

An auxiliary winding with N_2 turns number and opposed polarity is coupled to the storage inductor L_b with N_1 turns number. This auxiliary winding is used to discharge the storage inductor L_b when occurs an open circuit problem in the primary side of the transformer. Otherwise, high damage overvoltages may occur mainly in the controlled switches.

From the flyback converter criterion operating in the continuous conduction mode is determined the turns number N_2 as

$$N_2 \geq \frac{(1-D)}{D}\frac{Vo}{Vi}N_1. \tag{7}$$

C. Autotransformer Design

The high frequency autotransformer T must be designed for half active output power, and high magnetic flux density, B, because the current through the windings is continuous and with low ripple. The autotransformer turns ratio must be unitary. Thus,

$$P_T = \frac{Po}{2}, \tag{8}$$

where P_T is the active power processed by the autotransformer T, and Po is the output power of the converter.

D. Transformer Design

The isolated high frequency transformer Tr must be designed for the total active output power. The transformer turns ratio is taken from (1) and from characteristic curves shown in Fig. 4.

In order to reduce Eddy currents loss in the core, so as leakage inductance, the winding layers of the primary and the secondary of the transformer are mounted as the sandwich assembly [12]. The power of the isolation transformer is determined by

$$P_{Tr} = Po \ . \tag{9}$$

E. DC Current Blocking Capacitor

The DC current blocking capacitor avoids the saturation problem of the isolated transformer. This capacitor must be made of polypropylene due to its low internal resistance and AC polarity, because the total load current circulates through it. Considering a peak to peak voltage variation, and current circulation through it, the capacitance of the capacitor C_b can be determined by

$$C_b = \frac{I_{Lb\_avg}(1-D)}{2 f_s \Delta V_{Cb}}, \tag{10}$$

where ΔV_{Cb} is the peak to peak voltage variation across capacitor defined as

$$\Delta V_{Cb} = \xi \frac{Vo}{a}, \tag{11}$$

ILbavg is the average current circulating in the storage inductor L_b, ξ is an absolute value lower than 1 relative to the primary side voltage of the transformer T_r (in practical applications can be chosen between 0.05 to 0.15).

F. Current and Voltage Stresses in Switches S_1 and S_2

The RMS current through the switch S_1 that is equal to the switch S_2, considering a small current ripple through the storage inductor L_b, can be determined by

$$I_{S1\_rms} \cong I_{Lb\_avg} \sqrt{\frac{3}{4} - \frac{D}{2}} \ . \tag{12}$$

The maximum voltage across of switches S_1 and S_2, without considering the parasitic inductances that causes overvoltages, is almost equal to the primary side voltage of the isolated transformer. The voltage across the switches is dependent of the leakage inductance of the transformer T_r and other parasitic inductances. Therefore, a snubber circuit is recommended to limit such value. The maximum voltage stress across the controlled switches is given by

$$V_{S1} = V_{S2} \geq \frac{Vo}{a} . \tag{13}$$

G. Current and Voltage Stresses in Diodes D_1-D_4

The average current through the rectifier diodes D_1-D_4 is given by

$$I_{D1\_avg} \cong \frac{Io}{2} . \tag{14}$$

The maximum reverse voltage across of the rectifier diodes D_1-D_4, without considering overvoltages, is equal to the output voltage that is expressed by

$$V_{D1} \geq Vo \ . \tag{15}$$

H. Output Filter Capacitor Design

The capacitance of the output filter capacitor, for purely resistive load, can be determined by

$$Co \geq \frac{Io(2D-1)}{2 \Delta V o f_s} . \tag{16}$$

IV. Experimental Results

A. Specifications

This section presents experimental results from the proposed isolated boost converter using three-state switching cell. The experimental prototype was built accordingly the specifications shown in Table I.

TABLE I
SPECIFICATIONS OF THE ISOLATED DC-DC CONVERTER USING TSSC

Input Voltage Range	Vi	42 - 54 [V_{DC}]
Output Power	Po	1 [kW]
Output Voltage	Vo	400 [V]
Switching Frequency	f_s	25 [kHz]

The assumed design parameters are: the maximum boost inductor current ripple is ΔI_{Lb}=0.18I_{Lb_avg}, the transformer turns ratio is $a=Ns/Np=3$, the maximum fixed duty cycle of the switches for minimum input voltage is $D_{max}=0.70$, the coefficient to find DC current blocking capacitor is ξ = 0.1, and the output voltage ripple is $\Delta Vo=0.01Vo$.

The components used for experimental implementation are listed in Table II

TABLE II
PARAMETERS OF THE IMPLEMENTED CONVERTER

Diodes $D_1 - D_5$	HFA15PB60
Boost Inductor L_b	L_b = 70µH Core NEE-55/28/21 (Thornton Ipec) N1= 17 turns N2=80 turns
Output Filter Capacitors C_o	470µF / 450V (electrolytic)
Blocking Capacitor C_b	10uF/250V (polypropylene)
Switches S_1 - S_2	IRFP4227
High Frequency Transformer T_r	Core NEE-65/26 (Thornton Ipec) Np=17 turns Ns=51 turns
High Frequency Autotransformer T	Core NEE-42/20 (Thornton Ipec) NT1 = NT2 = 19 turns

B. Experimental Waveforms and Curves

Fig. 6 shows the measured input voltage Vi and current through the boost inductor L_b. As can be seen, the current drawn by the proposed converter presents a low current ripple, suitable for battery powered applications, where its requirement is relevant to improve its useful lifetime. It's also important to note that the current ripple frequency is double of the switching frequency.

Figs. 7 and 8 shows the voltage and current through the autotransformer windings. These waveforms are similar that concludes that a good current balance with very low current ripple is achieved.

Fig. 9 shows drain to source voltage and drain current in the switch S_1. The commutation detail of this waveform during the switch S_1 turn-on and turn off are shown in Fig. 10 and 11, respectively. As can be seen, the switch presents a suitable commutation reducing losses and higher frequency interferences.

Figs. 12 and 13 shows the voltages and currents through the primary side and secondary side of the isolated transformer T_r, respectively. It can be seen that the DC component of the primary side current is eliminated using the blocking capacitor C_b.

Finally, Fig. 14 presents the measured converter efficiency curve as a function of the output power. Accordingly to this graph evaluation, this converter presented a good efficiency that can be optimized if better devices were used. A picture of the developed prototype is shown in the Fig. 15, where can be seen the power conversion stage.

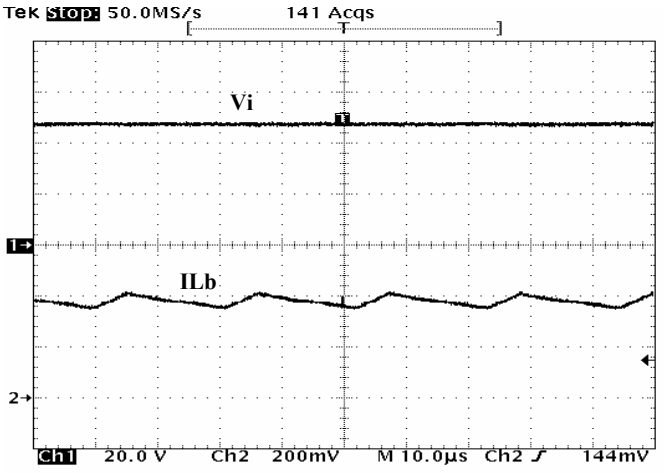


Fig. 6. Input voltage and current through the inductor Lb.
(20V/div.; 10A/div.; 10us/div.)

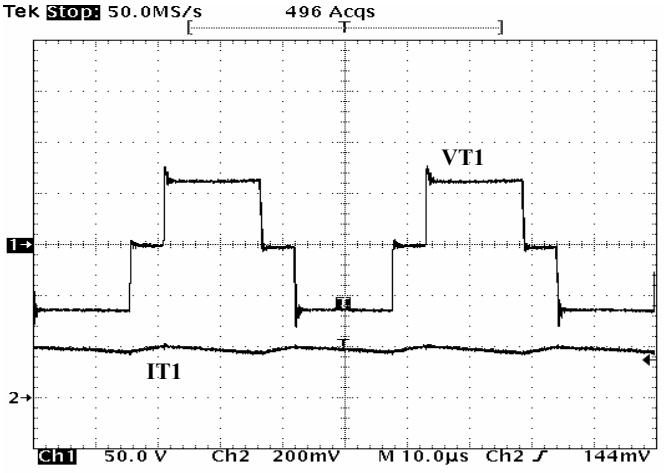


Fig. 7. Voltage and current through the autotransformer winding 1.
(50V/div.; 10A/div.; 10us/div.)

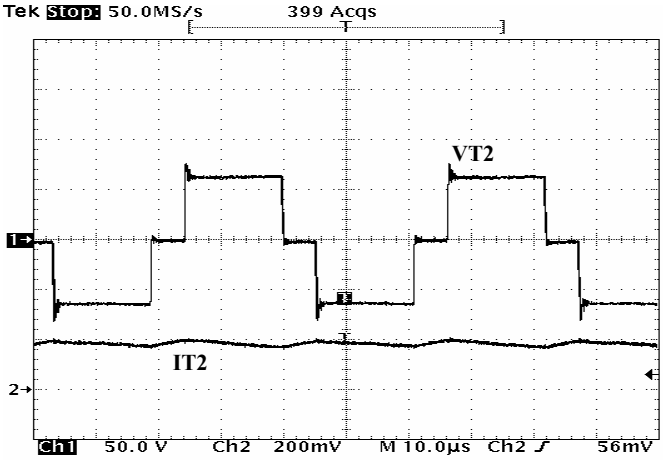


Fig. 8. Voltage and current through the autotransformer winding 2.
(50V/div.; 10A/div.; 10us/div.)

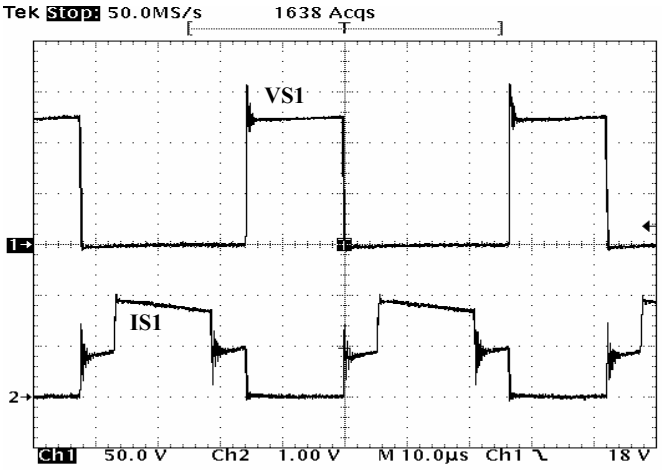


Fig. 9. Voltage and current through switch S_1.
(50V/div.; 10A/div.; 10us/div.)

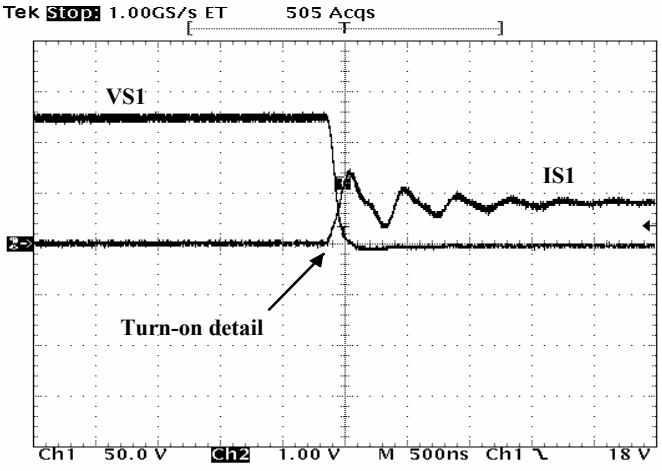


Fig. 10. Turn-on switching detail of the switch S_1.
(50V/div.; 10A/div.; 500ns/div.)

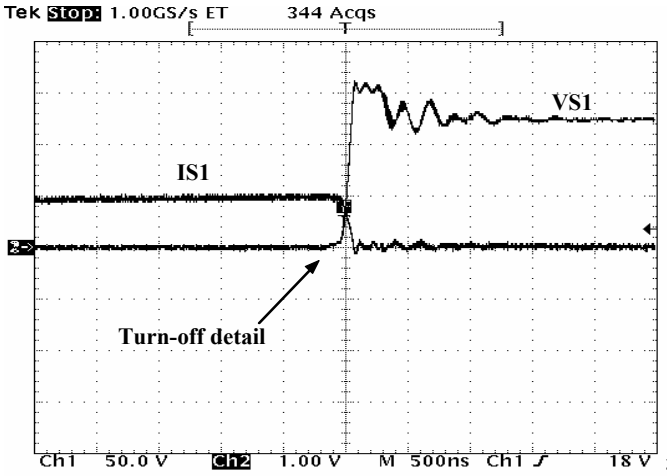


Fig. 11. Turn-off switching detail of the switch S_1.
(50V/div.; 10A/div.; 500ns/div.)

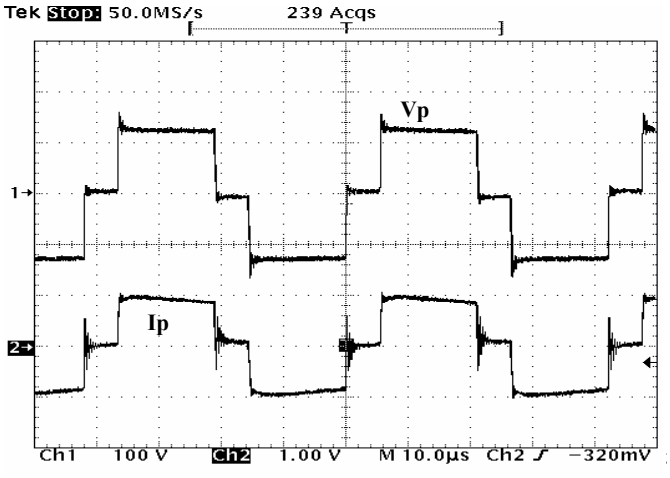


Fig. 12. Primary transformer voltage and current.
(100V/div.; 10A/div.; 10us/div.)

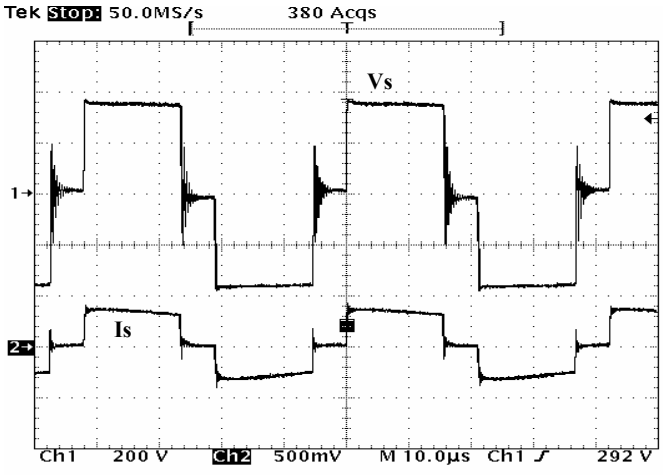


Fig. 13. Secondary transformer voltage and current.
(200V/div.; 5A/div.; 10us/div.)

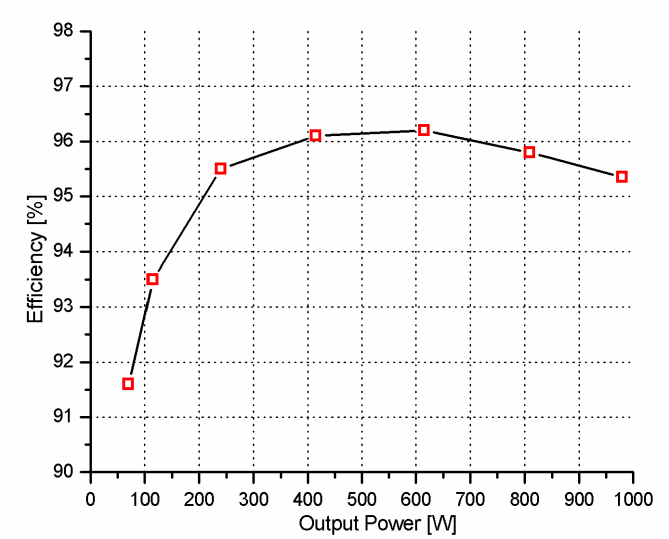


Fig. 14. Measured efficiency of the converter as function of the output power.

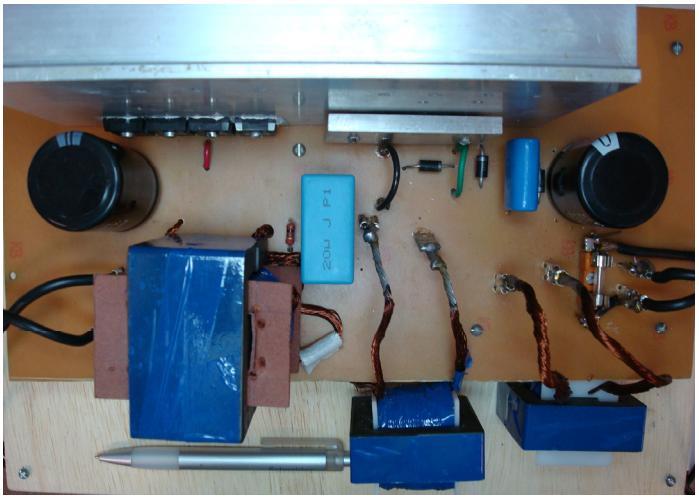


Fig. 15. Picture of the assembled prototype.

V. CONCLUSION

This paper presented a new isolated DC-DC boost converter based on the three-state cell (3SSC). Accordingly to the obtained experimental results, the major features that are important to emphasize are: lower blocking voltages across the controlled switches which allows the utilization of MOSFETs switches with lower drain-to-source resistances, the DC current across isolated transformer could be eliminated using blocking capacitor, and the reasonable leakage inductance value of the isolated transformer is suitable for commutation of the controlled switches. Thus, a high efficiency of the converter was obtained (up to 95.2%) for a full load condition.

Compared to the previous proposed topologies for the same purpose, this proposal is a competitive alternative for practical applications. It's important to note that if the design is optimized it could also increase its efficiency.

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