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Image Processing System With Multiple DSPs

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An image processing system is described using digital signal processors to perform pixel level data processing at maximum speed. The system is based on the VMEbus and consists on a number of modules working under the control of a host computer. Images are digitized by an acquisition module and transmitted to several processing modules by an interconnecting video bus. Each processing module operates on a region of the image implementing in this way a SIMD computing architecture. Finally an image acquisition and processing module is discussed which is being developed around a very recent 32-bit signal processor.

1. INTRODUCTION

In real-time digital image processing the speed required by most applications and the large quantity of data to process preclude the use of conventional computers in this task. Dedicated architectures have been used [1-2], but they offer little flexibility and require a considerable effort in their programming. In order to solve these problems the image processing system illustrated in Figure 1 was designed. The configuration shown is for still image coding and, as can be seen, it operates under the control of a VMEbus host computer. To allow fast transfers of the images the modules are connected through a video bus carrying digitized images from left to right.

The module on the left, the video acquisition module, is responsible for a number of functions and must be allways present in the system. The essential function of the video controller module is to drive the video address lines of the video bus. These addresses are used by all the modules in the system and define the (x,y) pixel position in an image when the image is scanned line by line from left to right and from top to bottom. Another function of the module is to digitize the video signal of a TV camera or an equivalent sensor, and send the digitized image samples and corresponding addresses to the video bus. Finally the module has the capacity of displaying the stored image in a colour monitor.

The modules numbered 1 to N in Figure 1 are called image processing modules and have the capability to process images appearing in their input video ports. The modules can be configurated either to pass the incoming video digital samples to their video output port with minimum delay or they can transmit the processed image in their local memory to other modules further to the right. The first case is the normal mode of operation and in this mode the modules acquire and process images. In the second case a module transmits an image in the following way: when the processed image is ready to transmit, the module waits until the address of the first processed pixel appears on the video bus and then starts the transmission by driving the video bus through the output port.

This modular architecture allows flexible configurations adapted to particular tasks. In scene analysis an image can be partioned through several processing units each operating on a particular region of the image. This is equivalent to a SIMD (Single Instruction Multiple Data) architecture. Each image processing module is based on a digital signal processor

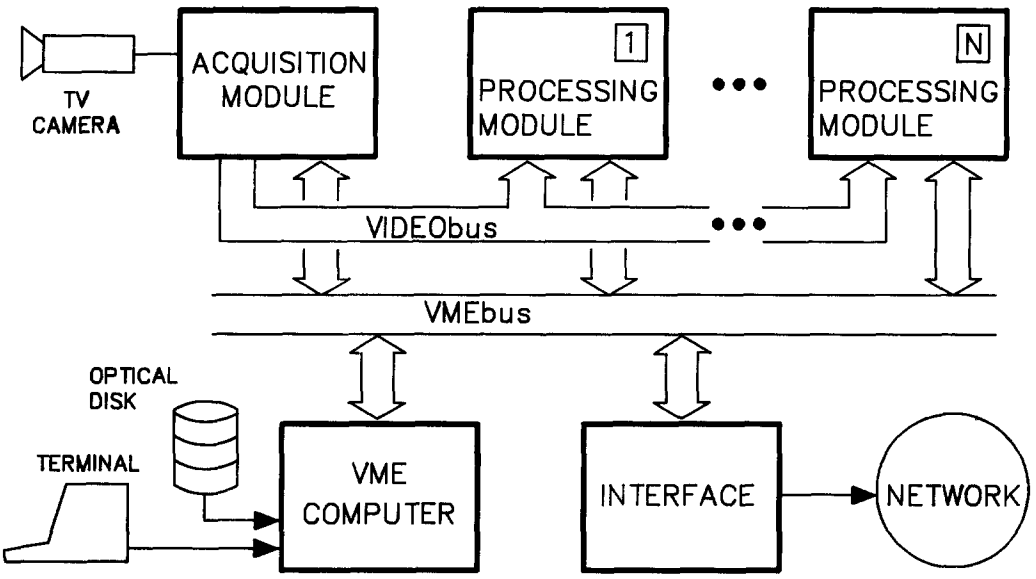

FIGURE 1

Block diagram of a digital image processing system composed of several DSP based processing modules operating on different parts of an image transmitted on the video bus. The configuration shown is for picture coding.

as described in the next section. The module spends one frame to acquire an image, one or more frames to process it, and one frame to transmit the image to other modules. The block diagram in Figure 1 was used with 4 identical processing units to compress still pictures using the algorithm of block transform coding [3]. In comparison to a conventional image processing system composed of a single VME frame-grabber operated by a 68020 CPU, this system is approximately 40 times faster. This reduction is a consequence of two factors. Firstly we perform parallel processing by distributing the computations by 4 different processing modules. Secondly we achieve a further 10 times reduction by using special processors (TMS32025) with special instructions for image processing.

2. SYSTEM DESCRIPTION

A more detailed illustration of the proposed image processing architecture is shown in Figure 2. In this section we describe the video bus, the acquisition and display module, and the DSP-based image processing module.

2.1 Video Bus

The video bus is an uni-directional bus transporting the digitized video from the acquisition module to the modules on the right.

For a 512x512 image resolution obtained from a TV camera, samples are converted at a sampling period of 68ns which is a very short time considering the transmission through the video bus. In order to increase the fiability of the bus and to allow for slower logic in the processing modules, two 8-bit video samples are packed in a single 16-bit word and this word is transmitted at a rate of 136ns. Therefore the video bus transports 2 samples every cycle on 16 data lines.

In relation to the pixel addresses of the 512x512 image mentioned above, 17 lines are needed to specify one out of 256x512 pairs of

pixels travelling on the video bus, giving a total number of 34 lines if we count an extra signal for validation. This is the number of lines driven by the acquisition module. In the case of the processing modules, 68 connections would be required since the signals are both inputs and outputs. For practical reasons [4], the address signals are not duplicated. Instead, they are externally delayed as shown in Figure 2. This brings the number of connections at a processing module down to 54.

2.2. Acquisition and Display Module

The acquisition and display module is a self-contained unit whose main function is to drive the video bus with pixel addresses. In addition it provides the interface of the image processing system to standard black and white TV cameras using the CCIR norm, and to conventional black and white or colour monitors. We describe the module referring to the block diagram shown in Figure 2. As it can be seen up to four video inputs can be connected to this module which uses a flash 8-bit analog to digital converter to digitize the selected channel. The display section of the module uses a conventional CRT controller and a colour look-up table which incorporates three 6-bit digital to analog converters to generate a RGB video signal with 256 colours from a palette of 256,144.

The acquisition module has the capacity to store two complete images of 512x512 pixels on its internal 512K bytes of RAM memory organized as two 256K bytes frame buffers. Although the video memory is accessible by the CPU on a pixel basis, allowing image processing by the host, this is not the normal working situation. In fact a major feature of the module is the capability of sending the digitized video to the local memory of the image processing modules present in the system.

When activated by the host, the video bus interface section of the module sends two samples of video data, and their corresponding addresses, every 136ns. The video bus interface of this module continually presents valid addresses and a strobe signal to be used by all modules in the system.

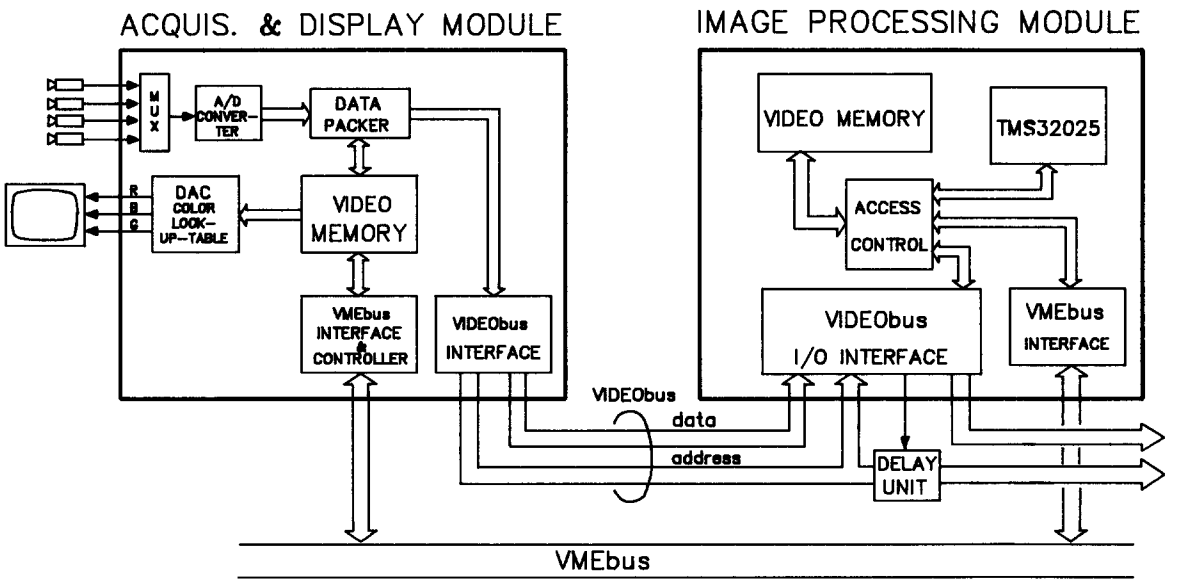

FIGURE 2

Diagrams of the acquisition and of the image processing modules. The video bus carries the digitized video samples and the corresponding addresses.

2.3. Image Processing Module

As shown in Figure 2 the module is composed of four parts: a video input and output section, a DSP microprocessor (TMS32025), the memory for program and image data and a VMEbus interface. The video section uses the video bus addresses in two ways. When programmed by the host computer to receive an image, it uses the incoming address to write the digitized video into its local memory. If the module is programmed to transmit an image, the referred to addresses are used to move the processed pixels from the memory to the video output port. Under the command of the host computer, the video input module may be configured to acquire images of different sizes (windows) on different picture positions.

The chosen digital signal processor is a 16-bit microprocessor [5] working at 40 MHz with a 100ns instruction cycle. In this design the local intelligence of the module is in the DSP which is totally controlled by the VME host computer. All the memory of the DSP, both program memory and data image memory, is RAM and appears in the address map of the host. In this way, the host may halt the DSP processor, download a program or a command, activate the reception or emission of a picture through the Video bus and return control to the DSP processor for the execution of a command.

The maximum program memory of the TMS32025 is 64k words but only 32k words are used in this application. For data memory (a total of 256K bytes) a paginated system enables the addressing of all the data using eight pages of 32K bytes. The TMS32025 accesses this video data on the top of the memory where it only finds 8 valid bits in each location instead of the usual 16-bit word. The alternative of storing two video samples per word is not efficient from a programming point of view.

The VME interface module permits the access to the video memory, the TMS 32025 program memory and the control registers of the image processing module. To avoid conflicts in accessing the shared memory, a priority access controller was included in the module.

3. A NEW DESIGN FOR IMAGE PROCESSING

A module for image processing having both acquisition and processing capabilities is presently under development. This design uses a novel microprocessor, the TMS32030, which is fully exploited. In relation to the previous microprocessor used in the module described in section 2.3, this processor has a large memory space, a 60ns instruction cycle and two separate 32-bit wide external buses [6]. These facts allow the inclusion of the processor in the video acquisition module replacing many of the logic circuits used in its control.

As shown in Figure 3 the processor clock is synchronized to the horizontal synchronism extracted from the incoming video signal. This is achieved by using one of the internal timers of the processor to perform the equivalent function of a divider in a phase-lock-loop (PLL). The timer is programmed such that the instruction cycle of the processor equals the pixel convertion time of the A/D converter (68ns). This is fundamental for the processor to control the acquisition and display sections of the module. The processor has three modes of operation: acquisition, processing and display, as next explained.

In the acquisition mode the processor reads 4 pixels packed in a 32-bit wide word and transfers the data to the video memory. The transfer has to be completed in four instruction cycles and is done in software. This is possible by a number of reasons. Firstly, a single instruction can move data from one external bus to the other, providing that the instruction is fetched from the processor on-chip program memory and that it is preceeded by the "repeat n" intruction. Secondly, the video memory can be dynamically organized either as 32-bit wide or 8-bit wide words. In the acquisition mode (and display) the memory appears as 32-bit words each containing four 8-bit pixels.

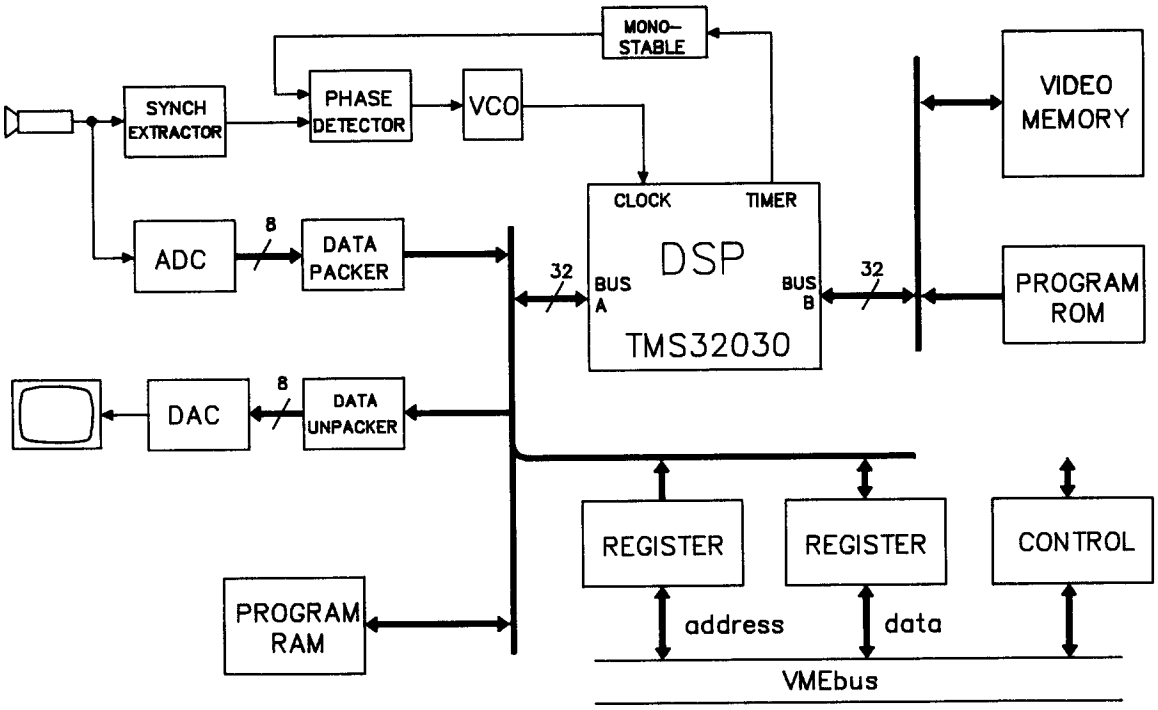

FIGURE 3

Block diagram of a general purpose image processing system based on the 32-bit TMS32030 digital signal processor. The processor can control all the operations of the module, since it is synchronized to the video signal.

Finally, the transfer instruction can be used with an addressing mode in which the register containing the destination address is automatically incremented by four.

In the processing mode the DSP works on the video memory which is configurated as an 8-bit wide memory. This is done by the inclusion of data buffers (not shown in the figure) which link the 8 least significant data bus lines of the processor to the proper memory bank. When in this mode, the host computer may access the video and program memory by generating either "write" or "read" interrupts in different interrupt lines of the processor. In response the processor reads the register containing the memory address, moves data to or from the host data register and acknowledges the cycle according to the host protocol.

In the display mode the DSP transfers data in a similar way as in the acquisition mode, moving data from the video memory to the D/A converter data unpacker. The main difference is that the accesses from the host are allowed in this mode, instead of being ignored as in the acquisition mode.

An important aspect of this design is the existence of a block of RAM on the external peripheral bus (A in the figure). This block is intended to contain program code loaded from the host. Because the video memory is placed on the other external bus (bus B in the figure), this permits a maximum throughput due to the existence of many TMS32030 "parallel" instructions that transfer, in the same cycle, different data on the two external buses.

4. CONCLUSION

An image processing computing architecture has been described allowing great flexibility and improved performance. The high performance of this system results from the modular approach of the design and from the inclusion of a digital signal processor in each image processing module. A general purpose image processing module based on a novel digital signal processor has also been discussed. Further work is under way to design a new video bus to fully support the capabilities of this processor.

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